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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,559	12/29/2003	Justin K. Brask	P18244	9088

7590 03/03/2005

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/748,559	BRASK ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *17-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/29/03,06/01/04,09/24/04, 09/27/04, 12/21/04*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-16 in the reply filed on 08 Feb. 2005 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by US6475908 to Lin et al.

Regarding claim 1, Lin discloses a method for making a semiconductor device in fig. 6-11 comprising: forming a NMOS gate electrode 62, column 5 line 65, on a first part of a substrate 100; and forming a silicide PMOS gate electrode 72, column 5 line 66, on a second part of the substrate, fig. 11.

Regarding claim 2, Lin discloses the method wherein the first part of the substrate comprises a first gate dielectric layer 60, column 5 line 44, and the second part of the substrate comprises a second gate dielectric layer 60, fig. 11.

Regarding claim 3, Lin discloses the method wherein the first and second gate dielectric layers 60 comprises silicon dioxide, column 5 line 37.

Regarding claim 4, Lin discloses the method wherein the first gate dielectric layer 60 comprises a high-k gate dielectric layer, column 5 line 38, and the second dielectric layer 60 comprises silicon dioxide, column 5 line 37.

Regarding claims 6-7, Lin discloses the method wherein the metal NMOS gate electrode 62 comprises a material that is selected from the group consisting of titanium, cobalt and nickel column 5 line 45, wherein the silicide PMOS gate electrode 72 comprises a material selected from the group consisting of nickel silicide, cobalt silicide, and titanium silicide, table 1.

Regarding claim 8, Lin discloses the method wherein the metal NMOS gate electrode 62 has a workfunction that is between about 3.9 eV and about 4.2 eV, and the silicide PMOS gate electrode 72 has a midgap workfunction that is between about 4.3 eV and about 4.8 eV, table 1.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over US6475908 to Lin et al. in view of US 6794306 to Kim et al.

Regarding claim 5, Lin discloses the method wherein the high-k dielectric layer 60 comprises a material selected from the group consisting of hafnium oxide, column 5 line 40.

But Lin does not disclose the method wherein the high-k dielectric layer 60 is formed by atomic layer chemical vapor deposition.

However, Kim discloses the method wherein the hafnium oxide high-k gate dielectric layer 24 is formed by atomic layer chemical vapor deposition (CVD), column 5 line 61-62. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the atomic layer CVD teaching of Kim to form a high-k dielectric layer in Lin's method, because it would have a good step coverage as taught by Kin, column 5 line 62.

7. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6858483 to Doczy et al. in view of US 6835639 to Rotondaro et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome

by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claim 9, Doczy discloses a method for making a semiconductor device comprising: forming a first polysilicon layer (n-type poly), fig. 1, which is bracketed by a pair of sidewall spacer, fig. 1, on a first gate dielectric layer, fig. 1, and a p-type polysilicon layer, fig. 1, on a second gate dielectric layer; removing the first polysilicon layer, fig. 3, to generate a trench that is positioned between the pair of sidewall spacers, fig. 3; forming an n-type metal layer 405, fig. 4, within the trench.

But Doczy does not disclose the method converting substantially all of the p-type polysilicon layer to a silicide.

However, Rotondaro discloses the method converting substantially all of the PMOS polysilicon layer, column 3 line 59 fig. 2, to a silicide, column 3 line 26. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the PMOS silicide gate teaching of Rotondaro with Doczy's method, because it would have created a CMOS with different work function as taught by Rotondaro, see abstract. Furthermore, Lin is also disclosing the different work function of metal and silicide gates for NMOS and PMOS in fig. 11 and table 1.

Regarding claim 10, Doczy does not disclose the method wherein the first gate dielectric layer and the second gate dielectric layer each comprise silicon dioxide and wherein the first polysilicon layer and the p-type polysilicon layer are each between about 100 and about 2,000 angstroms thick.

However, Rotondaro discloses the method wherein the first gate dielectric layer and the second gate dielectric layer each comprise silicon dioxide, column 3 line 14, and wherein the first polysilicon layer and the p-type polysilicon layer are each between about 1000 angstroms thick, column 3 line 59. Accordingly, it would have been obvious to one of ordinary skill in art to use the thickness teaching of Rotondaro with Doczy's method in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 11, Doczy discloses the method wherein a wet etch process that is selective for the first polysilicon layer over the p-type polysilicon layer is applied to remove the first polysilicon layer, column 2 line 19-22.

Regarding claim 12, Doczy discloses the method wherein the N-type metal layer comprising a material that is selected from the group consisting of hafnium, zirconium, tantalum, aluminum, and metal carbide, column 2 line 28

But, Doczy does not disclose the method wherein all of the p-type polysilicon layer is converted to a silicide.

However, Rotondaro discloses the method converting substantially all of the PMOS polysilicon layer, column 3 line 59 fig. 2, to a silicide, column 3 line 26. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the PMOS silicide gate teaching of Rotondaro with Doczy's method, because it would have created a CMOS with different work function as taught by Rotondaro, see abstract. Furthermore, Lin is also disclosing the different work function of metal and silicide gates for NMOS and PMOS in fig. 11 and table 1.

8. Claims 13, 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6858483 to Doczy et al. in view of US 6835639 to Rotondaro et al and US 6475908 to Lin et al.

Regarding claim 13, Doczy discloses the method for making a semiconductor device comprising: forming an n-type polysilicon layer, fig. 1, which is bracketed by a pair of sidewall spacers, fig. 1, on a first gate dielectric layer, and a p-type polysilicon

layer on a second gate dielectric layer, fig. 1, applying a wet etch process that is selective for the n-type polysilicon layer over the p-type polysilicon layer to remove the n-type polysilicon layer, fig. 3 column 2 line 19-22, without removing significant portions of the p-type polysilicon layer, fig. 3, generating a trench that is positioned between the pair of sidewall spacers, and exposing the first gate dielectric layer, fig. 3, forming an n-type metal layer 405, fig. 4, on the gate dielectric layer to generate a metal NMOS gate electrode, fig. 8.

But Doczy does not disclose the method wherein removing the exposed first gate dielectric layer, forming a high-k gate dielectric layer on the substrate at the bottom of the trench, and converting the p-type polysilicon layer to a silicide to generate a silicide PMOS gate electrode.

However, Lin discloses the method forming a NMOS wherein removing the exposed first gate dielectric layer 42, column 5 line 14, fig. 7, forming a high-k or low-k gate dielectric layer 60, column 5 line 35-39, on the substrate 10 at the bottom of the trench, fig. 8. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use the method of forming high-k gate dielectric for NMOS teaching of Lin with Doczy's method, because such dielectric substitution would have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06.

With respect to silicide PMOS gate electrode, Rotondaro discloses the method converting substantially all of the PMOS polysilicon layer, column 3 line 59 fig. 2, to a silicide, column 3 line 26. At the time the invention was made; it

would have been obvious to one of ordinary skill in the art to use the PMOS silicide gate teaching of Rotondaro with Doczy's method, because it would have created a CMOS with different work function as taught by Rotondaro, see abstract. Furthermore, Lin is also disclosing the different work function of metal and silicide gates for NMOS and PMOS in fig. 11 and table 1.

Regarding claims 15-16, Doczy discloses the method wherein the wet etch process comprises exposing the n-type polysilicon layer to an aqueous solution that includes between about 2 and about 30 percent of a source of hydroxide by volume, column 2 lines 20-25, wherein the source of hydroxide comprises a compound that is selected from the group consisting of ammonium hydroxide, column 2 line 21.

9. Claims 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6858483 to Doczy et al., US 6835639 to Rotondaro et al and US 6475908 to Lin et al. as applied to the above claim 13 in further in view of US 6794306 to Kim et al.

Regarding claim 14, Doczy discloses the method wherein the n-type metal layer comprises a mate/al that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and metal carbide, column 2 line 28.

But Doczy does not disclose the high-k gate dielectric layer is foced by atomic layer chemical vapor deposition, and comprises a material selected from the group consisting of hafnium oxide, and the silicide comprises a material selected from the group consisting of nickel silicide, cobalt silicide, and titanium silicide.

However, Kim discloses the method wherein the hafnium oxide high-k gate dielectric layer 24 is formed by atomic layer chemical vapor deposition (CVD), column 5 lines 61-62. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the atomic layer CVD teaching of Kim to form a high-k dielectric layer in Lin's method, because it would have a good step coverage as taught by Kim, column 5 line 62.

With respect to PMOS cobalt silicide gate electrode, Rotondaro discloses the method converting substantially all of the PMOS polysilicon layer, column 3 line 59 fig. 2, to a cobalt silicide, column 8 line 61. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the PMOS cobalt silicide gate teaching of Rotondaro with Doczy's method, because it would have created a CMOS with different work function as taught by Rotondaro, see abstract. Furthermore, Lin is also disclosing the different work function of metal gate and silicide gates, respectively, in fig. 11 and table 1.

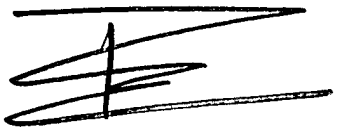
Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao X. Le
Patent Examiner
28 Feb. 2005